FIG. 1

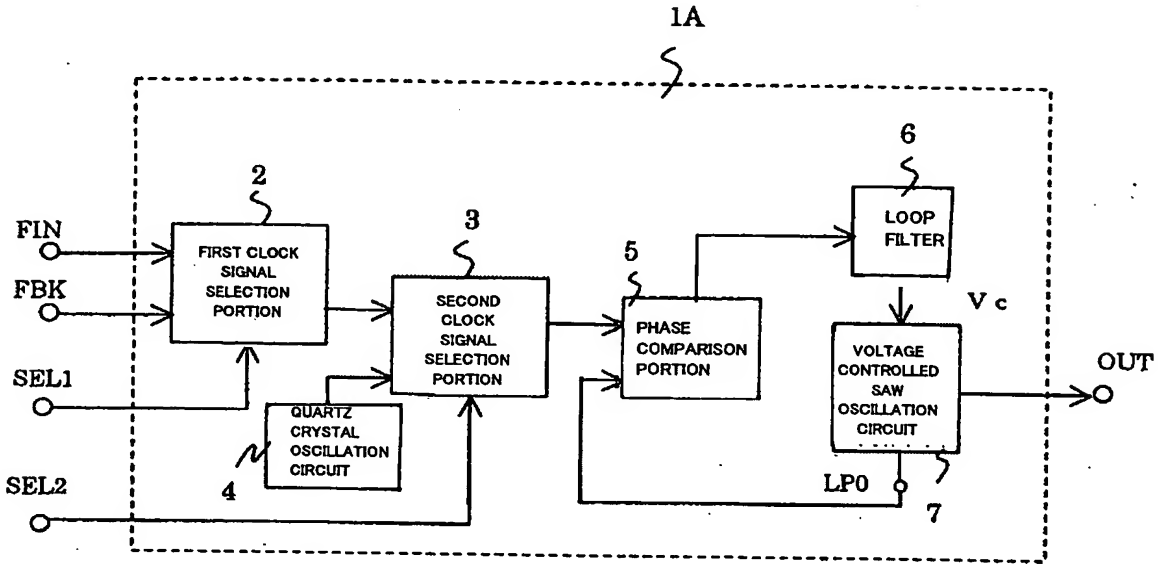



FIG. 2

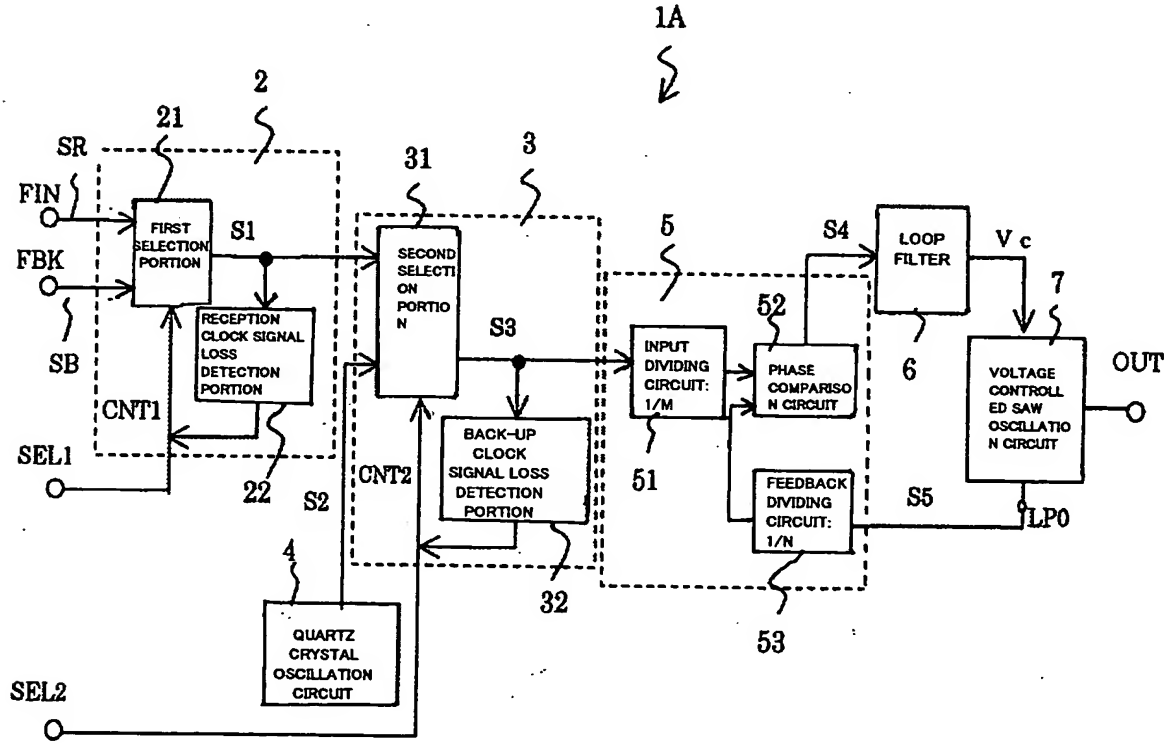
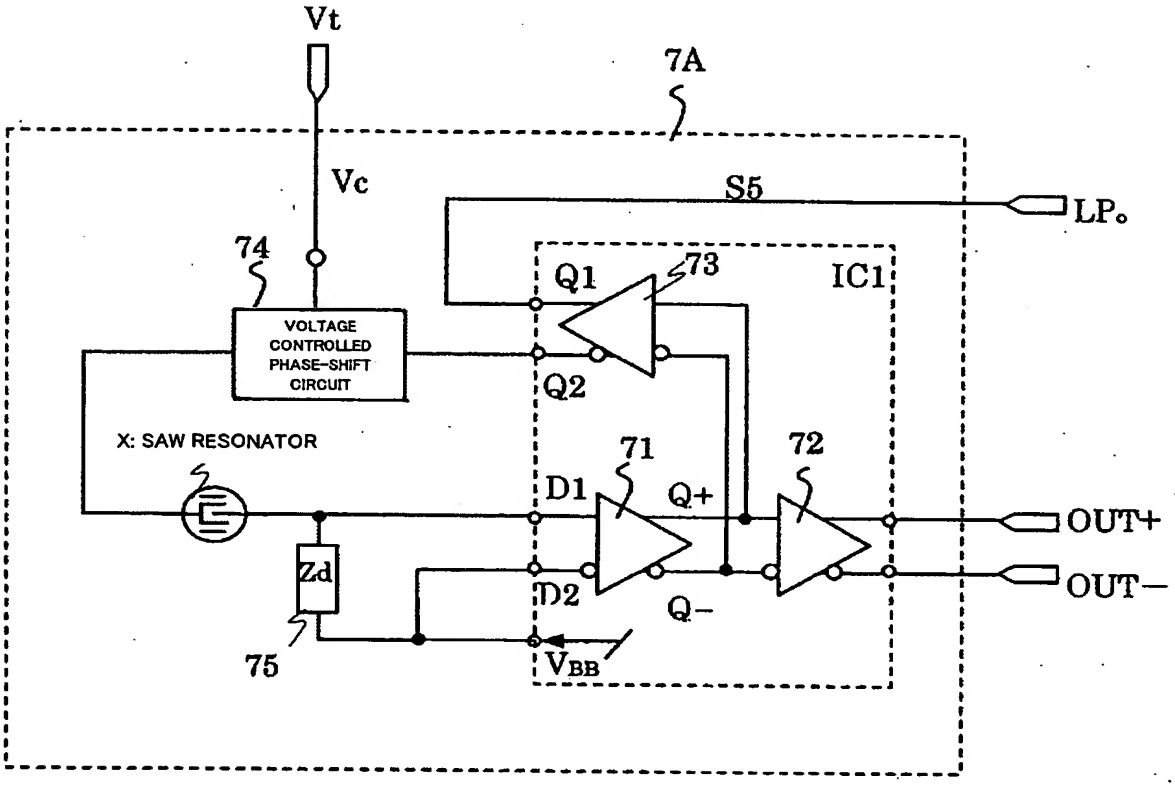


FIG. 3


Vt
7A
Vc
S5
LPo
74
Q1
73
IC1
VOLTAGE CONTROLLED PHASE-SHIFT CIRCUIT
Q2
X: SAW RESONATOR
71
72
D1
Q+
OUT+
Zd
D2
Q−
OUT−
75
VBB

F I G. 4

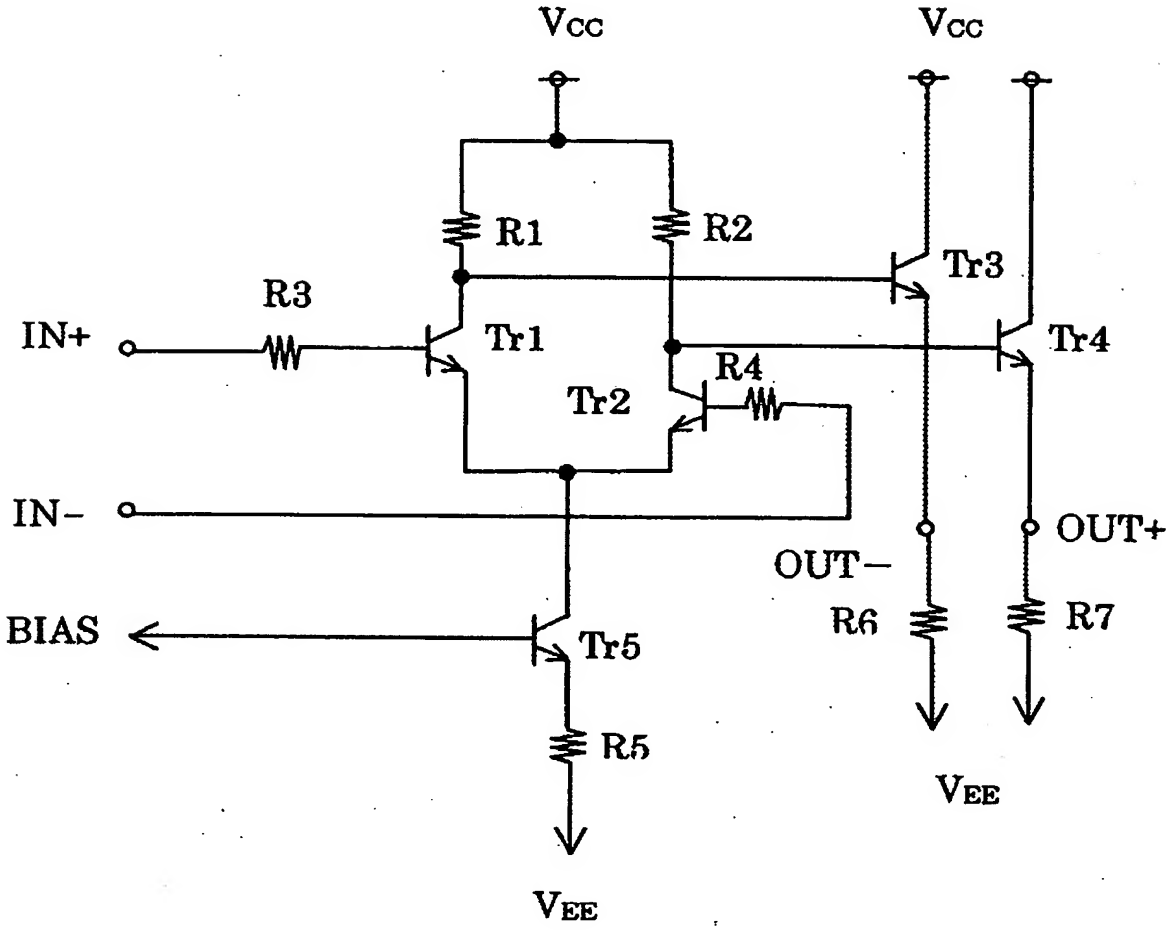
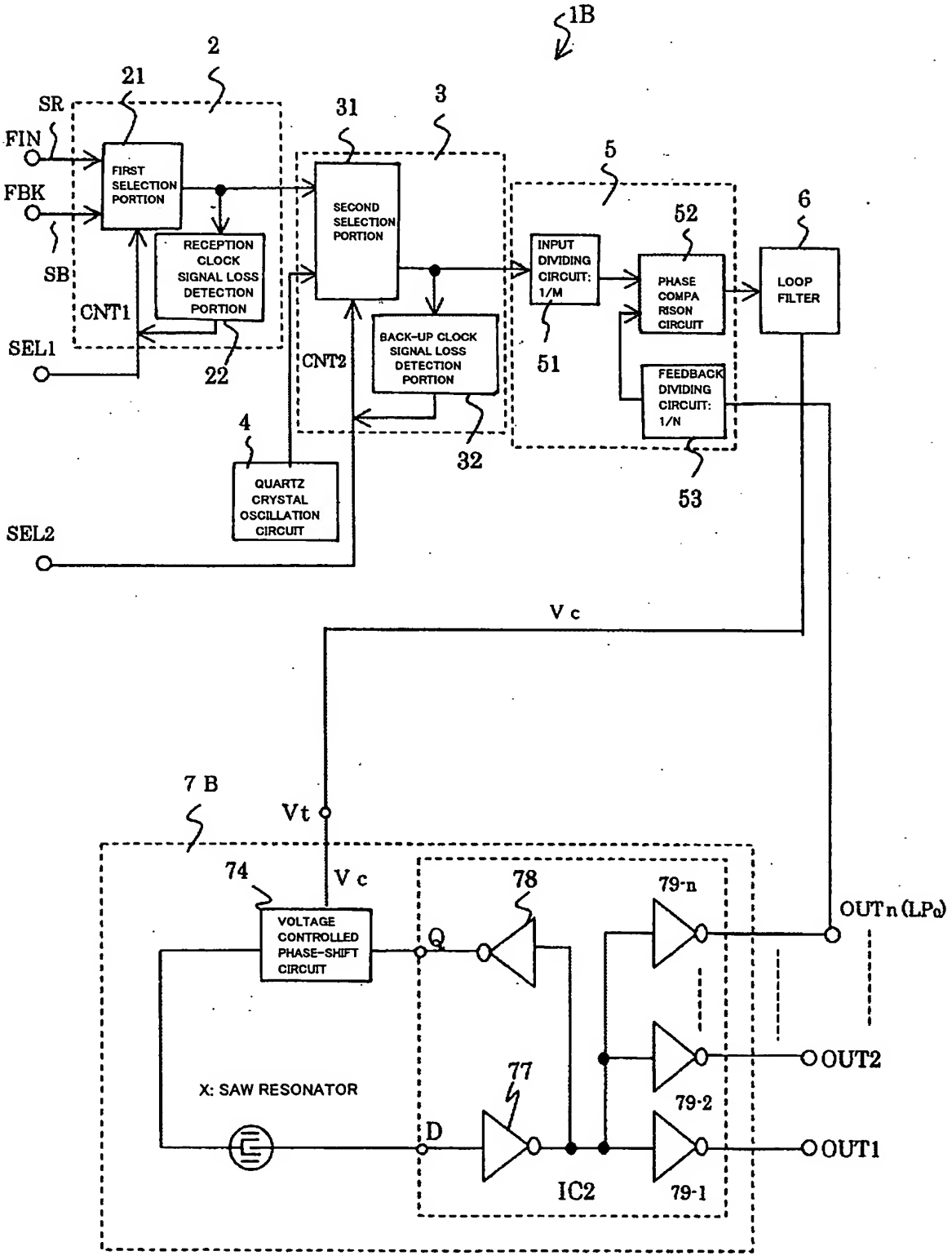
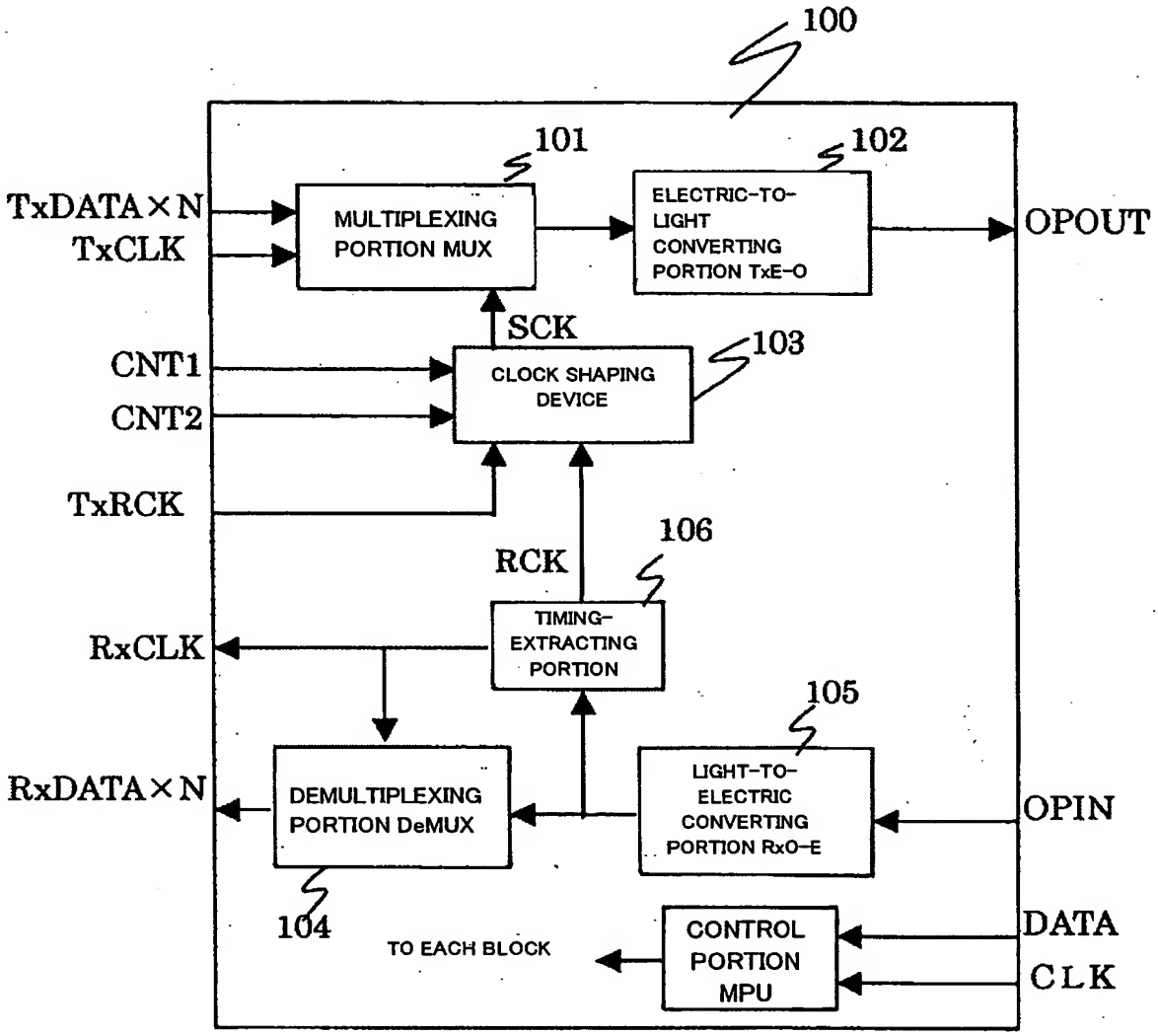

Vcc
Vcc
R1
R2
Tr3
R3
IN+
Tr1
Tr4
R4
Tr2
IN−
OUT+
OUT−
BIAS
R6
R7
Tr5
R5
VEE
VEE

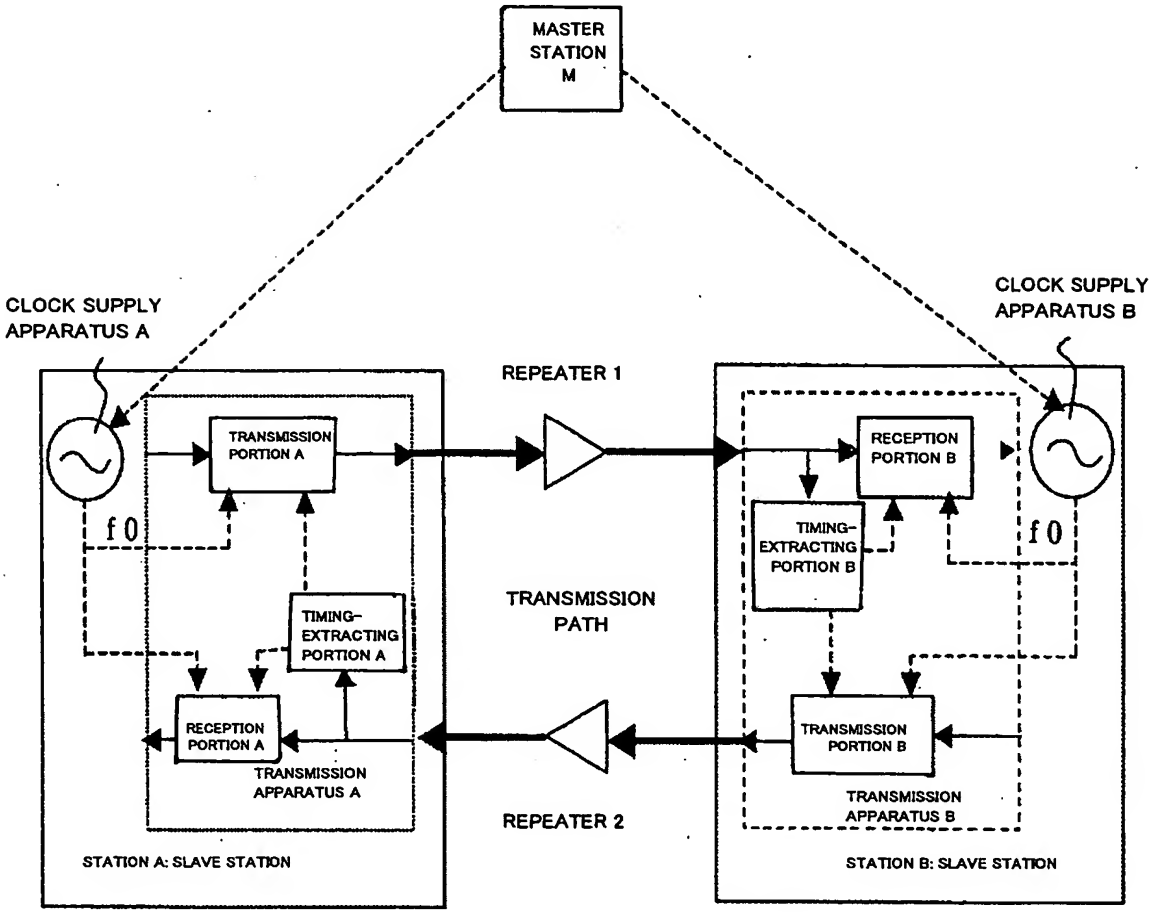
FIG. 5


1B
2
21
SR
FIN
FBK
SB
FIRST SELECTION PORTION
RECEPTION CLOCK SIGNAL LOSS DETECTION PORTION
CNT1
SEL1
22
31
3
SECOND SELECTION PORTION
CNT2
BACK-UP CLOCK SIGNAL LOSS DETECTION PORTION
32
4
QUARTZ CRYSTAL OSCILLATION CIRCUIT
SEL2
5
INPUT DIVIDING CIRCUIT: 1/M
51
52
PHASE COMPARISON CIRCUIT
FEEDBACK DIVIDING CIRCUIT: 1/N
53
6
LOOP FILTER
Vc
7B
Vt
74
Vc
VOLTAGE CONTROLLED PHASE-SHIFT CIRCUIT
Q
78
79-n
OUTn (LPe)
X: SAW RESONATOR
77
D
79-2
OUT2
OUT1
IC2
79-1

F I G. 6


100
101
102
TxDATA×N
TxCLK
MULTIPLEXING PORTION MUX
ELECTRIC-TO-LIGHT CONVERTING PORTION TxE-O
OPOUT
SCK
CNT1
CNT2
CLOCK SHAPING DEVICE
103
TxRCK
RCK
106
TIMING-EXTRACTING PORTION
RxCLK
105
RxDATA×N
DEMULTIPLEXING PORTION DeMUX
LIGHT-TO-ELECTRIC CONVERTING PORTION RxO-E
OPIN
104
TO EACH BLOCK
CONTROL PORTION MPU
DATA
CLK

F I G. 7


MASTER STATION M
CLOCK SUPPLY APPARATUS A
CLOCK SUPPLY APPARATUS B
REPEATER 1
TRANSMISSION PORTION A
RECEPTION PORTION B
f0
f0
TIMING-EXTRACTING PORTION B
TIMING-EXTRACTING PORTION A
TRANSMISSION PATH
RECEPTION PORTION A
TRANSMISSION PORTION B
TRANSMISSION APPARATUS A
TRANSMISSION APPARATUS B
REPEATER 2
STATION A: SLAVE STATION
STATION B: SLAVE STATION

F I G. 8

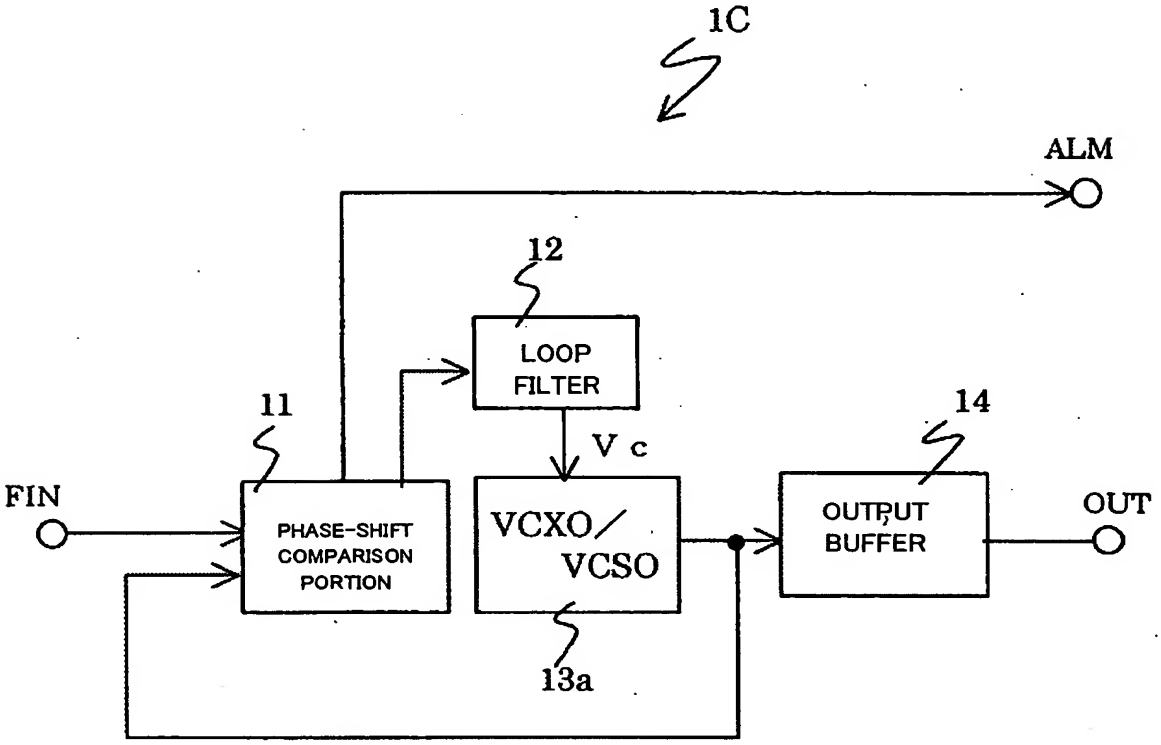

1C
ALM
12
LOOP
FILTER
11
14
Vc
FIN
PHASE-SHIFT
COMPARISON
PORTION
VCXO/
VCSO
OUTPUT
BUFFER
OUT
13a

FIG. 9

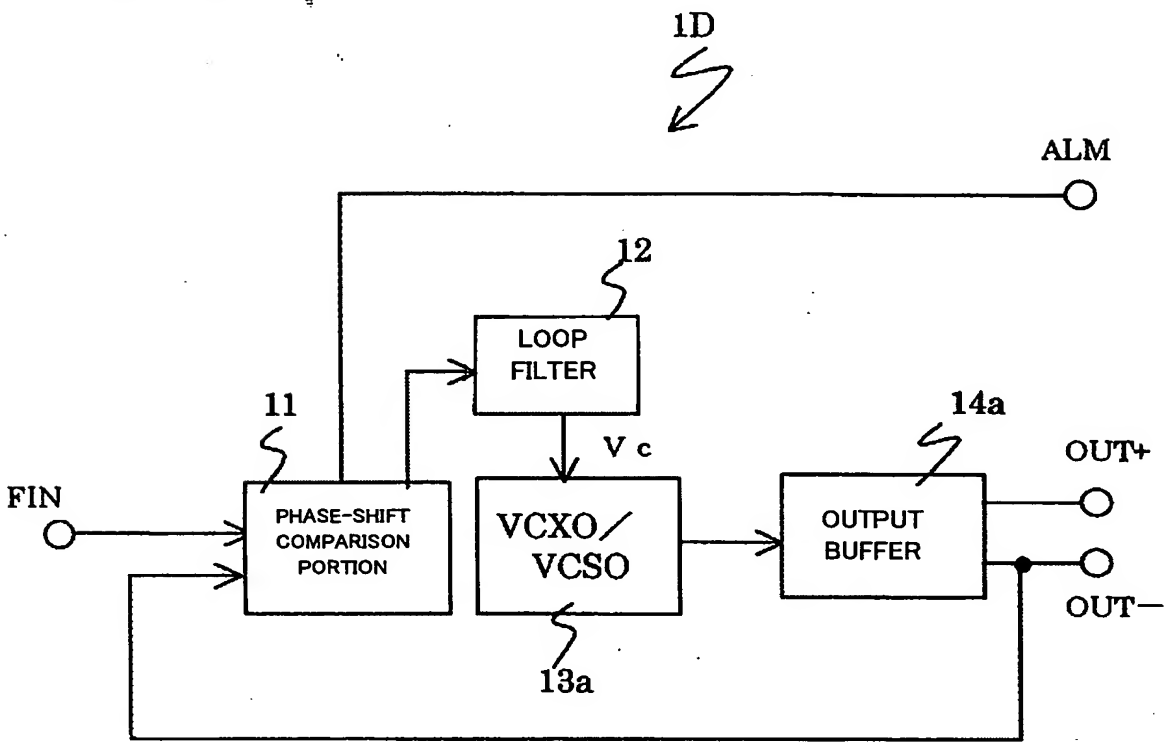
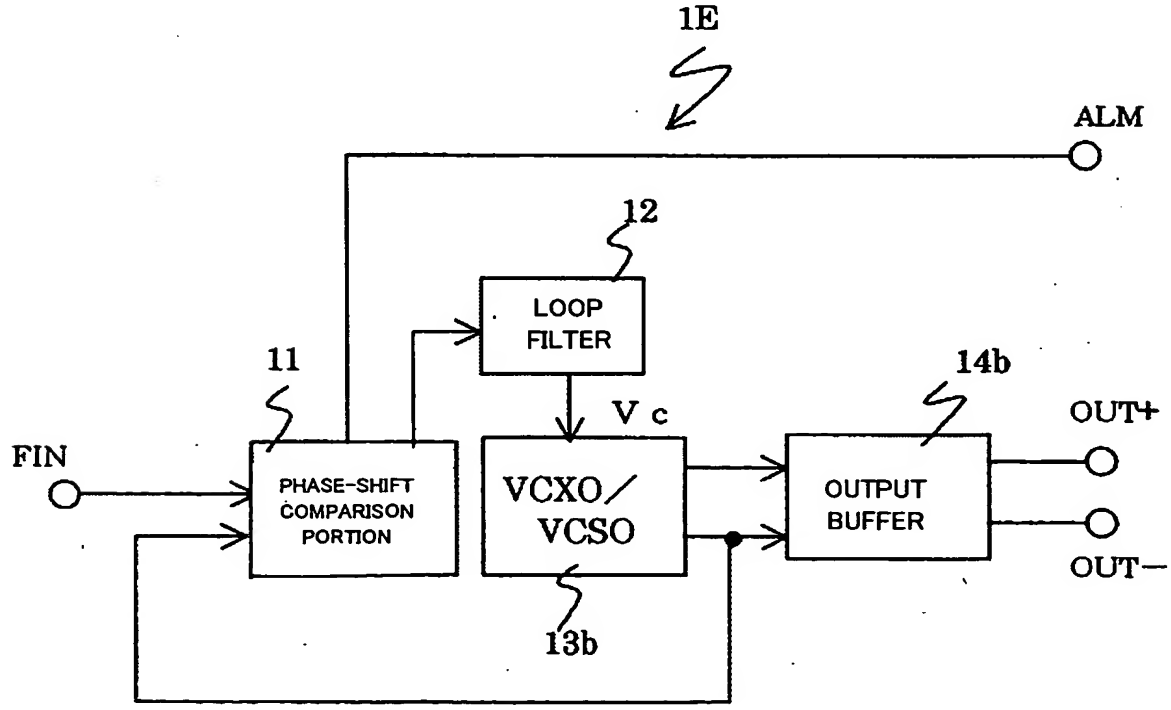

1D
ALM
12
LOOP FILTER
11
14a
Vc
OUT+
FIN
PHASE-SHIFT COMPARISON PORTION
VCXO/ VCSO
OUTPUT BUFFER
OUT−
13a

FIG. 10


1E
ALM
12
LOOP FILTER
11
14b
Vc
OUT+
FIN
PHASE-SHIFT COMPARISON PORTION
VCXO/ VCSO
OUTPUT BUFFER
OUT−
13b